WHAT IS CLAIMED IS:

1. An information processing unit, comprising a plurality of processors in one chip, wherein said plural processors execute an instruction independently, and wherein said each processor comprises a decoder circuit for determining the instruction to be executed uniquely, based on input history of instruction codes, by an instruction code inputted thereto from a plurality of instructions which are assigned to the instruction code.

2. The information processing unit according to claim 1, wherein said decoder circuit holds a prescribed information corresponding to the input history of the instruction codes and determines the instruction to be executed uniquely based on the information as well as the instruction code inputted thereto.

3. The information processing unit according to claim 1, further comprising an instruction to which the optional instruction code is assigned.

4. The information processing unit according to claim 1, further comprising an instruction which is determined by the instruction code inputted thereto, regardless of the input history of the instruction codes.

5. An information processing unit, comprising a plurality of processors which execute instructions independently in one chip, wherein the instructions

executable by said processor are sorted into a plurality of groups of instructions, with instruction codes which are different from each other in the same group being added to each instruction, wherein said processor selects the group of instruction corresponding to the instruction code inputted thereto based on the input history of the instruction code to determine the instruction uniquely by the instruction code inputted thereto.

6. An information processing unit, comprising a plurality of processors which execute instructions independently in one chip, wherein the instructions executable by said processor are sorted into a plurality of groups of instructions indicated by a group code, with the instruction codes which are different from each other in the same group of instruction being added to each instruction, and wherein said each processor comprises a decoder circuit which determines the instruction to be executed uniquely based on said group code corresponding to input history of the instruction codes and the instruction code inputted thereto, and a processor element which executes an operation corresponding to a control signal supplied from said decoder circuit.

7. The information processing unit according to claim 6, wherein said each processor further comprises a group resister which stores the group

codes set on the basis of the input history of said instruction code.

8. The information processing unit according to claim 7, wherein said each processor further comprises a look up table which defines the rule for changing the group code stored in said group register.

9. The information processing unit according to claim 8, wherein said look up table defines a combination of an instruction mask for setting bit to be masked, an instruction code for comparing the instruction with the internal instruction code generated by the group code and the input instruction code, and a changed group code.

10. The information processing unit according to claim 6, wherein the instruction executable by said processor includes an alias instruction which assigns in advance the optional instruction for the internal instruction code generated by the group code and the input instruction code.